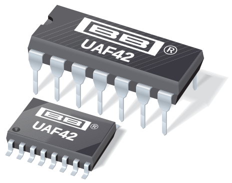


UAF42

UNIVERSAL ACTIVE FILTER

FEATURES

- VERSATILE—
  LOW-PASS, HIGH-PASS
  BAND-PASS, BAND-REJECT
- SIMPLE DESIGN PROCEDURE
- ACCURATE FREQUENCY AND Q — INCLUDES ON CHIP 1000pF ±0.5% CAPACITORS

APPLICATIONS

- TEST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION SYSTEMS
- MONOLITHIC REPLACEMENT FOR UAF41

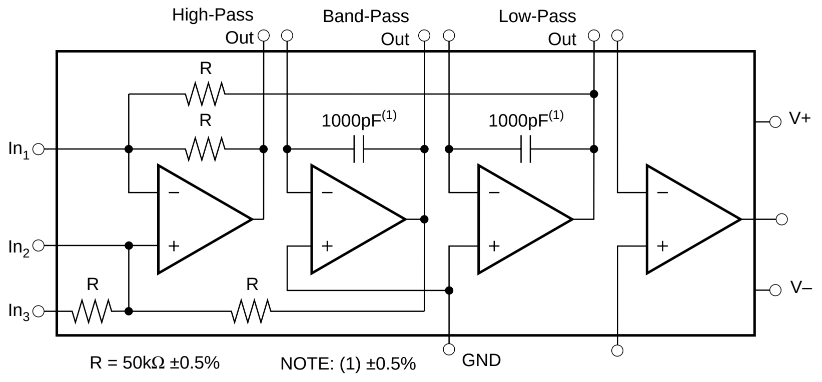
DESCRIPTION

The UAF42 is a universal active filter which can be configured for a wide range of low-pass, high-pass, and band-pass filters. It uses a classical state-variable analog architecture with an inverting amplifier and two integrators. The integrators include on-chip 1000pF capacitors trimmed to 0.5%. This solves one of the most difficult problems of active filter design—obtaining tight tolerance, low-loss capacitors.

A DOS-compatible filter design program allows easy implementation of many filter types such as Butterworth, Bessel, and Chebyshev. A fourth, uncommitted FET-input op amp (identical to the other three) can be used to form additional stages, or for special filters such as band-reject and Inverse Chebyshev.

The classical topology of the UAF42 forms a time-continuous filter, free from the anomalies and switching noise associated with switched-capacitor filter types.

The UAF42 is available in 14-pin plastic DIP and SOL-16 surface-mount packages, specified for the –25°C to +85°C temperature range.



R = 50kΩ ±0.5%   NOTE: (1) ±0.5%

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PDS-1070H

Printed in U.S.A. January, 1998

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

		UAF42AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
FILTER PERFORMANCE					
Frequency Range, fn			0 to 100		kHz
Frequency Accuracy	f = 1kHz			1	%
vs Temperature			0.01		%/°C
Maximum Q			400		—
Maximun (Q • Frequency) Product			500		kHz
Q vs Temperature	$(f_O \cdot Q) < 10^4$		0.01		%/°C
	$(f_O \cdot Q) < 10^5$		0.025		%/°C
Q Repeatability	$(f_O \cdot Q) < 10^5$		2		%
Offset Voltage, Low-Pass Output				±5	mV
Resistor Accuracy			0.5	1%	%
OFFSET VOLTAGE(1)					
Input Offset Voltage			±0.5	±5	mV
vs Temperature			±3		μV/°C
vs Power Supply	V_S = ±6 to ±18V	80	96		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		10	50	pA
Input Offset Current	V_{CM} = 0V		5		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			25		$nV/\sqrt{Hz}$
f = 10kHz			10		$nV/\sqrt{Hz}$
Voltage Noise: BW = 0.1 to 10Hz			2		μVp-p
Input Bias Current Noise					
Noise Density: f = 10kHz			2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE(1)					
Common-Mode Input Range			±11.5		V
Common-Mode Rejection	V_{CM} = ±10V	80	96		dB
INPUT IMPEDANCE(1)					
Differential			10^{13} || 2		Ω || pF
Common-Mode			10^{13} || 6		Ω || pF
OPEN-LOOP GAIN(1)					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	90	126		dB
FREQUENCY RESPONSE(1)					
Slew Rate			10		V/μs
Gain-Bandwidth Product	G = +1		4		MHz
Total Harmonic Distortion	G = +1, f = 1kHz		0.0004		%
OUTPUT(1)					
Voltage Output	R_L = 2kΩ	±11	±11.5		V
Short Circuit Current			±25		mA
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±6		±18	V
Current			±6	±7	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

✻ Same as specification for UAF42AP.

NOTES: (1) Specifications apply to uncommitted op amp, A_4. The three op amps forming the filter are identical to A_4 but are tested as a complete filter.

PIN CONFIGURATION

NOTE: NC: No Connection. For best performance connect all “NC” pins to ground to minimize inter-lead capacitance.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	$\pm V_S$ ±0.7V
Output Short Circuit	Continuous
Operating Temperature:	
Plastic DIP, P; SOIC, U	–40°C to +85°C
Storage Temperature:	
Plastic DIP, P; SOIC, U	–40°C to +125°C
Junction Temperature:	
Plastic DIP, P; SOIC, U	+125°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
UAF42AP	Plastic 14-pin DIP	010	–25°C to +85°C
UAF42AU	SOL-16	211	–25°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

APPLICATIONS INFORMATION

The UAF42 is a monolithic implementation of the proven state-variable analog filter topology. Pin-compatible with the popular UAF41 Analog Filter, it provides several improvements.

Slew Rate of the UAF42 has been increased to 10V/µs versus 1.6V/µs for the UAF41. Frequency • Q product of the UAF42 has been improved, and the useful natural frequency extended by a factor of four to 100kHz. FET-input op amps on the UAF42 provide very low input bias current. The monolithic construction of the UAF42 provides lower cost and improved reliability.

DESIGN PROGRAM

Application Bulletin AB-035 and a computer-aided design program, available from Burr-Brown, make it easy to design and implement many kinds of active filters. The DOS-compatible program guides you through the design process and automatically calculates component values.

Low-pass, high-pass, band-pass and band-reject (notch) filters can be designed. The program supports the three most commonly used all-pole filter types: Butterworth, Chebyshev and Bessel. The less-familiar Inverse Chebyshev is also supported, providing a smooth passband response with ripple in the stop-band.

With each data entry, the program automatically calculates and displays filter performance. This allows a spreadsheet-like "what if" design approach. For example, you can quickly determine, by trial and error, how many poles are required for a desired attenuation in the stopband. Gain/phase plots may be viewed for any response type.

The basic building element of the most commonly used filter types is the second-order section. This section provides a complex-conjugate pair of poles. The natural frequency, ω_n, and Q of the pole pair determines the characteristic response of the section. The low-pass transfer function is

$$\frac{V_O(s)}{V_I(s)} = \frac{A_{LP}\omega_n^2}{s^2 + s\,\omega_n/Q + \omega_n^2} \qquad (1)$$

The high-pass transfer function is

$$\frac{V_{HP}(s)}{V_I(s)} = \frac{A_{HP}s^2}{s^2 + s\,\omega_n/Q + \omega_n^2} \qquad (2)$$

The band-pass transfer function is

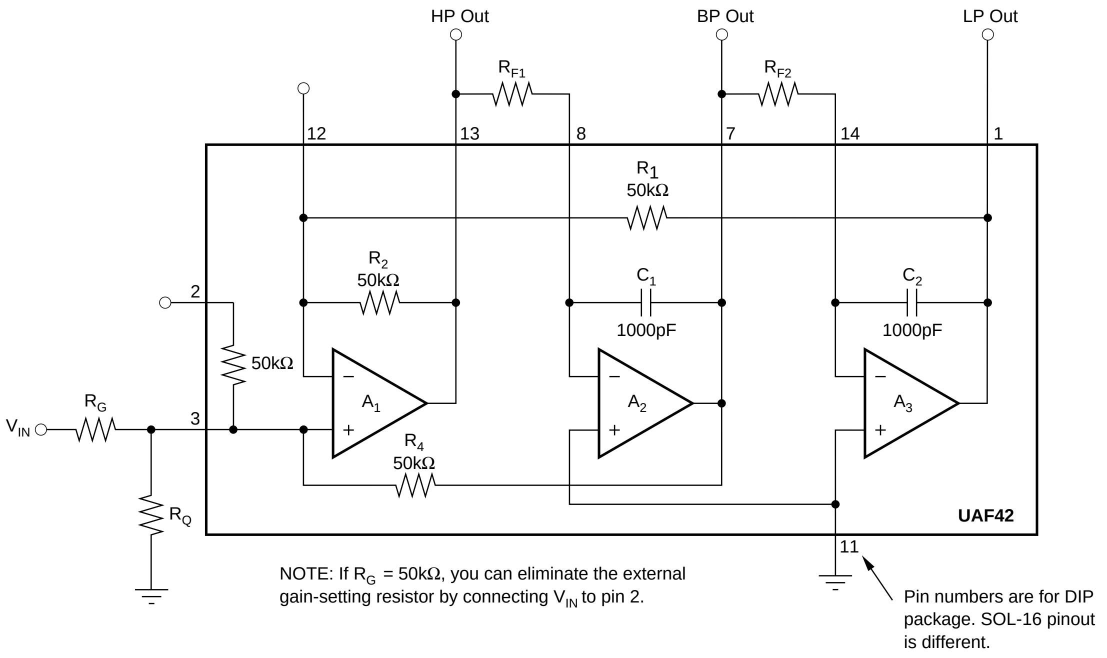
$$\frac{V_{BP}(s)}{V_I(s)} = \frac{A_{BP}(\omega_n/Q)\;\; s}{s^2 + s\,\omega_n/Q + \omega_n^2} \qquad (3)$$

A band-reject response is obtained by summing the low-pass and high-pass outputs, yielding the transfer function

$$\frac{V_{BR}(s)}{V_I(s)} = \frac{A_{BR}(s^2 + \omega_n^2)}{s^2 + s\,\omega_n/Q + \omega_n^2} \qquad (4)$$

The most commonly used filter types are formed with one or more cascaded second-order sections. Each section is designed for ω_n and Q according to the filter type (Butterworth, Bessel, Chebyshev, etc.) and cutoff frequency. While tabulated data can be found in virtually any filter design text, the design program eliminates this tedious procedure.

Second-order sections may be non-inverting (Figure 1) or inverting (Figure 2). Design equations for these two basic configurations are shown for reference. The design program solves these equations, providing complete results, including component values.



NOTE: If R_G = 50kΩ, you can eliminate the external gain-setting resistor by connecting V_{IN} to pin 2.

Pin numbers are for DIP package. SOL-16 pinout is different.

Design Equations

1. $$\omega_n^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$$

2. $$Q = \frac{1 + \dfrac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \dfrac{R_2}{R_1}} \left(\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2} \right)^{1/2}$$

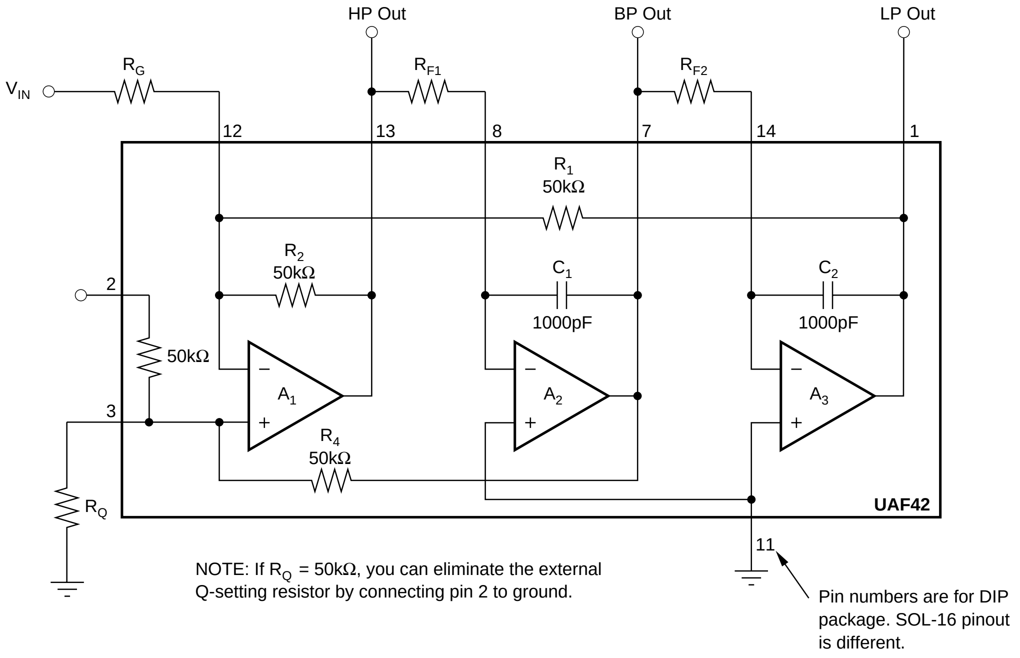
3. $$QA_{LP} = QA_{HP} \left(\frac{R_1}{R_2} \right) = A_{BP} \left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2} \right)^{1/2}$$

4. $$A_{LP} = \frac{1 + \dfrac{R_1}{R_2}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4} \right)}$$

5. $$A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{1 + \dfrac{R_2}{R_1}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4} \right)}$$

6. $$A_{BP} = \frac{R_4}{R_G}$$

FIGURE 1. Non-Inverting Pole-Pair.



NOTE: If $R_Q = 50k\Omega$, you can eliminate the external Q-setting resistor by connecting pin 2 to ground.

Pin numbers are for DIP package. SOL-16 pinout is different.

Design Equations

1. $$\omega_n^2 = \frac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$$

2. $$Q = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)} \left(\frac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$$

3. $$QA_{LP} = QA_{HP}\left(\frac{R_1}{R_2}\right) = A_{BP}\left(\frac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$$

4. $$A_{LP} = \frac{R_1}{R_G}$$

5. $$A_{HP} = \frac{R_2}{R_1} A_{LP} = \frac{R_2}{R_G}$$

6. $$A_{BP} = \left(1 + \frac{R_4}{R_Q}\right) \frac{1}{R_G\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$$

FIGURE 2. Inverting Pole-Pair.

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